2048x2048 VISIBLE/INFRARED HgCdTe FOCAL PLANE ARRAYS (FPAs)

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ABSTRACT

Rockwell has developed the world's largest multiplexer for use with infrared HgCdTe and visible silicon detector arrays. The resulting FPAs are to be proposed for the Next Generation Space Telescope (NGST) program, ground-based astronomy, and other low background applications. The 2048x2048 multiplexer's unit cell size is 18 µm x 18 µm with source follower per detector input (SFD) and 4 and 32 output amplifier selections. SWIR detectors with a spectral response of 0.85 µm to 2.5 µm have been processed on liquid phase epitaxy (LPE) HgCdTe on sapphire substrates. MWIR detectors (0.85-5.0 µm) will be processed on molecular beam epitaxy (MBE) HgCdTe on CdZnTe substrates. Response to wavelengths as low as 0.4 µm is possible with the substrate removal process and an example of this will be given. The multiplexer has been designed and fabricated at Conexant (formerly Rockwell Semiconductor Systems). Room temperature probing shows that the device is functional with excellent yield – 20%. Novel hybrid fabrication techniques have been used to construct the first engineering grade FPA, currently being tested. This HAWAII-2 device is based on the highly successful HAWAII 1024x1024 device and the performance will be similar. The ultimate performance expected from the array is: dark currents of <0.01 e-/s, quantum efficiency of >55% across the spectral band, and noise levels of <3 e- for the SWIR and <10 e- for the MWIR band using Fowler sampling. We expect to achieve these performance levels at 77K for the SWIR and >40K for the MWIR band. The first 2048x2048 hybrid has been fabricated and the results will be discussed. Also, high quantum efficiency (90%) and low dark current (0.1 nA/cm2 at 257K) silicon detectors have been fabricated and characterized. The electro-optical characteristics of these devices will be discussed. These devices may already have high enough radiation hardness for many space missions.

1 INTRODUCTION

Infrared FPA (IR FPA) technology, detector arrays and read-out integrated circuits, have made dramatic progress in the past 10 years, resulting in the most recent 2048x2048 pixel FPA success. Infrared focal plane array sizes have consistently increased due to advances in detector and CMOS multiplexer technologies, as well as detector array, hybridization, and packaging technologies. The multiplexers continue to "piggyback" on the tremendous advances in CMOS integrated circuit processing technology due to the commercial computer microprocessor and DRAM demands. The 2048x2048 HAWAII-2 multiplexer was fabricated using 0.8 µm design rules; this way, knowing that the 1024x1024 multiplexers could be yielded, lower risk was taken in terms of yield and operation.

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The first engineering grade HAWAII-2 was constructed with PACE-I detector[1] array technology. PACE-I was chosen because more than thirty 1024x1024 FPAs[2] employing PACE-I have been delivered worldwide, making it the lowest risk approach. For HAWAII-2, the source follower per detector (SFD) was the chosen as the best low risk approach, optimum for ground based astronomy applications. After the completion of the characterization and evaluation of the performance of the PACE-I based HAWAII-2 FPA, we plan to fabricate 5 µm cutoff Molecular Beam Epitaxy (MBE) HgCdTe on CdZnTe detector arrays. The backside of these detectors will be removed for thermal cycling reliability and visible light detection. The hybridization and packaging techniques are similar to the ones used for PACE-I. Progress on the 2048x2048 work will be reported here.

Silicon detector arrays with excellent QE and low dark current have been fabricated for hybridization to Rockwell's TCM6600 and TCM8600 multiplexer designs. This technology can be readily extended to the HAWAII-2, making it useful in the near-UV, visible, and near-IR regions of the spectrum. This technology will be described and some data will be discussed here.

This paper is broken down into several sections, describing the HAWAII-2 FPA. Section 2 describes the HAWAII-2 multiplexer, and the yield associated with the first silicon production run. Section 3 describes the detector array options that can be hybridized to the HAWAII-2 multiplexer. Section 4 describes the assembly and assembly options available for the HAWAII-2. Section 5 provides HAWAII data to demonstrate the expected performance of the 2048x2048 FPA. Section 6 shows the initial QE map from the first engineering grade HAWAII-2 FPA, currently being tested. Sections 7 and 8 are the conclusion and acknowledgements.

2 HAWAII-2 2048×2048 CMOS READOUT

The HAWAII-2 is a 4.19 million pixel readout with 18µm pixel pitch in 0.8µm CMOS. It is structured as four fully independent 1024x1024 quadrants where each quadrant supports single-output or eight-output operation. Each 2048x2048 thus supports 4-tap or 32-tap readout at frame rates up to approximately 15 Hz. Basic operation requires seven CMOS-level clocks, two 5V power supplies (one analog and one digital), one fixed dc bias and one variable dc bias. The device has low electroluminescence[5] (i.e., self-glow) by virtue of optimized design. The HAWAII-2 FPA dark current is expected to be detector-limited at <0.01 electrons per second.

2.1 READOUT ARCHITECTURE AND FABRICATION STRATEGY

The quadrant architecture facilitated the use of low-risk photolithography in conjunction with optical stitching to produce twelve large-area readouts on each 200 mm wafer with >20% defect-free yield. While wafer-scale photolithography with ~1 µm feature is sometimes used to make even larger devices, submicron lithography often constrains the maximum die size to ~2 cm per side. The 1024×1024 HAWAII readout, for example, is nearly the largest integrated circuit that can be made using a GCA wafer stepper; its area encompasses 3.8 cm^2 and a total of >3.4M transistors. Most available steppers have smaller fields; some newer steppers capable of supporting 0.25 µm processes have slightly larger fields. We chose to fabricate each 4 cm × 4 cm readout by abutting four photolithographic optical fields to create each circuit, as shown in Fig. 1. Each quadrant is accurately abutted to the others to <0.05µm.

Each HAWAII-2 multiplexer is an array of source followers and supporting MOSFET switches as shown in the simplified schematic diagram (Fig. 2). The signal voltage from each pixel in the array is read through cascaded source followers. The various MOSFET switches are appropriately enabled and disabled to perform pixel access, reset, and readout. As shown in Figure 2, the photodiode is connected to the gate of the first stage source follower. The reset transistor is also connected to the gate of the first stage source follower and is used to reset the photodiode after each read. The source output of the first stage is connected to the first stage bias transistor, resident in the column buffer area of the multiplexer, through the pixel access switch transistor. The bias transistor is successively shared by the 1024 elements in each column as each is read on a row-by-row basis. The column bus is connected to the gate of the second stage source follower which is biased through an external resistor. The first stage source follower is only biased during pixel readout, via the shared bias transistor, minimizing pixel amplifier glow. The HAWAII-2 has the capability of bypassing the second stage source follower, allowing direct access to the column bus for external amplifier connection, to eliminate second stage source follower glow.

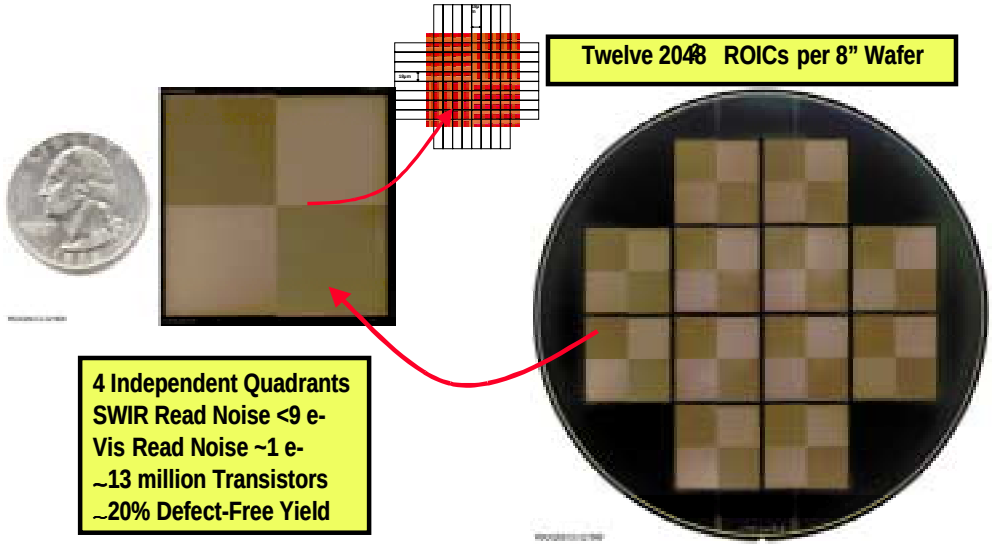


Figure 1. 2048x2048 CMOS Readout for IR astronomy is produced by photolithographically stitching four reticles with < 0.05 µm accuracy.

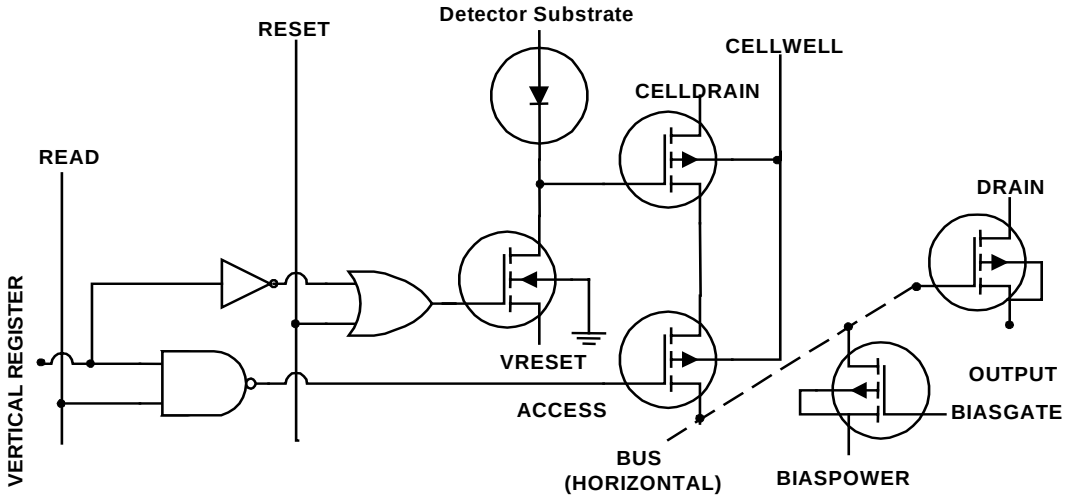


Figure 2. HAWAII-2: Key circuit elements including pixel and output buffer.

Though basic operation requires as few as seven clocks, up to ten clocks can be used to eliminate glow from the digital circuits and to facilitate an optional clocking mode that suppresses output amplifier non-uniformity. Since CMOS logic circuitry is used, the clock levels do not require precise adjustment for optimum performance. This simplified architecture also maximizes fabrication yield.

We have processed twenty-four wafers with twelve 2048x2048 die on each wafer. Six of these wafers have been probed at room temperature and the yields are shown in Fig. 3. Fourteen science grade devices (no rows or columns out) were yielded. Each quadrant in the FPA is completely independent. This makes it possible to yield useful devices with only one to three quadrants operational, making good 1024x 2048 or 1024x1024 FPAs from these parts. The 1024x 2048 or 1024x1024 quadrants can be diced out of a faulty 2048x2048 multiplexer, and used.

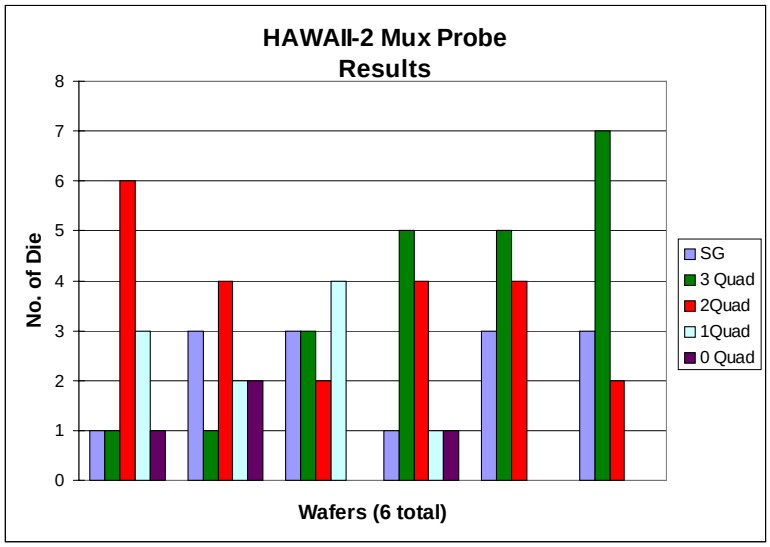


Figure 3. The 2048x2048 HAWAII-2 multiplexer room temperature probe results for six wafers. The science grade device yields, and devices with 1-3 quadrants working are shown.

2.2 MULTIPLE OPERATING MODES

In addition to several subtle design refinements relative to the predecessor 1024x1024 readout, the HAWAII-2 has several optional operating modes to enhance flexibility and performance. The basic mode provides one output per quadrant for a total of four outputs per FPA and a maximum frame rate of about 2 Hz. A second mode provides eight outputs per quadrant for a total of 32 outputs per FPA. The additional output taps boost the maximum frame rate to ~16 Hz to facilitate higher background signal iradiance and use with detectors at longer cutoff wavelengths. Since the composition of HgCdTe can be appropriately tuned, 5.5 µm 2048x2048 FPAs are feasible. The third mode also provides eight outputs per quadrant, but successively shuffles the video signals through each of the eight taps to suppress output amplifier offset nonuniformity. A fourth and final mode focuses on internal signal management; disabling this function operates the analog circuitry in a manner similar to the original HAWAII chip. Default operation, on the other hand, operates the device in a manner which should further lower the already low electrical crosstalk.

2.3 READOUT CHARACTERISTICS

Table 1 lists the expected characteristics of the HAWAII-2. The key differences between it and the 1024x1024 HAWAII include:

- slight reduction in pitch from 18.5 µm to 18 µm
- increase in die size from 19.8 mm by 19.8 mm to ≈39 mm by 39 mm.
- change to zero-insertion-force (ZIF) pin grid array (PGA) package from leadless chip carrier
- change from four-output readout to programmable four- or 32-output readout with optional fixed pattern noise suppression mode
- compatibility with order-of-magnitude higher background irradiance
- reference output added to each quadrant to enable lower drift via differential signal processing
- default mode reduces electrical crosstalk

Table 2 lists the clocks and biases needed to operate the FPA.

Table 1. HAWAII-2 Readout: Predicted Characteristics

Parameter	Minimum	Maximum	Units
Format	2048 × 2048		Pixels
Pixel Pitch	18		µm
Chip Package (Optional)	128 Pin		ZIF PGA
Die Size	≈39 x 39		mm^2
Input Circuit	Source Follower		
Temporal Noise Suppression	Off-chip: Correlated Double Sampling or Fowler Sampling		
Spatial Noise Suppression	8-Tap Video Averaging		
Supply Voltage	5		V
Integration Capacitance	20	35	10^{-15} F
Charge Capacity @0.5V	0.102	0.180	10^6 e-
Input Offset Nonuniformity		<5	mV p-p
Dynamic Range	>0.8	1	10^3
Output Taps	4	32	
Data Rate per Output Tap	1	≤2	MHz
Read Noise	<3	<9	e-
Conversion Gain (S_V)	≈3.5	≈7	µV/e-

Table 2. HAWAII-2: Clocks and biases

Input	Voltage (V)	Function
VDD, VDDA, BIASPOWER	5	Power Supplies
VSS, MUXSUB	0V	Multiplexer Ground
O1	Clock	Mode Control
O2	Clock	Mode Control
DRAIN	5/0	Output Amp Supply/Bus Output Select (5V Enable SF Out) (0V Enable Bus Out)
VRESET	0.5	Detector Reset Voltage
DSUB	0	Detector Common
CELLDRAIN	0	Analog Low in Unit Cell
BIASGATE	3.8	Sets SFD Current
VCLK	Clock	Fast Clock
LSYNC	Clock	Line Synchronization
CLK2	Clock	Line Clock 2
CLK1	Clock	Line Clock 1
CLKB2	Clock	Line Clock Bar 2
CLKB1	Clock	Line Clock Bar 1
FSYNC	Clock	Frame Synchronization
RESET	Clock	Pixel Reset Clock
READ	Clock	Pixel Read Clock
LRST	Clock	Output Shuffle Reset

2.4 DETECTOR INTERFACE CIRCUIT

The HAWAII-2 uses a source follower to read the photogenerated charge from each detector. This detector interface scheme works very well at low backgrounds, long frame times, and applications where MOSFET glow must be negligible compared to ultra-low detector dark current (~10^{-21} A). Photocurrent is integrated directly on the detector capacitance, so the detector must be reverse-biased to maximize dynamic range. SWIR detectors are

normally biased at from 0.5V to 1.0V. The detector voltage consequently changes with time under illumination and modulates the gate of a source follower whose drive FET is in the cell. The amplifier is only "on" during signal readout; this feature minimizes power dissipation and pixel amplifier glow. However, the limited size of this drive transistor constrains its ability to charge the bus capacitance and thus limits the electrical bandwidth. The overall gain reduction through the readout's two source follower stages is ~0.8 under nominal bias at 2 MHz data rate. The charge-handling capacity is approximately 100,000 electrons at 0.5V detector bias.

2.5 READ NOISE

The source follower per detector circuit is capable of very low read noise when the detector capacitance is small and the photoconversion gain is high. Assuming that correlated double sampling is employed off-chip, the percentage of background-limited infrared performance (BLIP), η_{BLIP}, is approximately:

$$\eta_{BLIP} = \frac{\left(\eta A_{\det} Q_B \tau_{\text{int}}\right)^{1/2}}{\left[\eta A_{\det} Q_B \tau_{\text{int}} + \frac{2kT\tau_{\text{int}}}{qR_{\det}} + N_{amp}^2 + \frac{2kT\tau_{\text{int}}}{qR_{rst}}\right]}$$

where R_{rst} is the off resistance of the reset FET. The dominant read noise of the source follower is:

$$N_{amp} \approx \frac{\sqrt{2}}{S_v}\left[\int^{\Delta f} V_n^2(f)\frac{\left[1-\cos(2\pi f t)\right]}{\left[1+(2\pi f T_D)\right]}df\right]^{1/2}$$

where $V_n(f)$ is the MOSFET noise as a function of frequency, T_D is the correlated double sampler time constant given by $T_D=t/2$, Δf is the measurement bandwidth and S_v is the readout conversion gain in units of V/e-. If correlated multiple sampling techniques are not used, the read noise will instead be dominated by the kTC noise generated from resetting the total input capacitance comprising the detector, indium bump, and source follower gate.

Assuming that the HAWAII-2 multiplexer will have $V_n(f)$ of roughly 2 μV/Hz$^{1/2}$ at 1 Hz (i.e., the same as HAWAII), a 1 sec integration time, 34 fF capacitance, and external electronics noise of 35 μV rms, the predicted HAWAII-2 read noise is about 7.3 e- with CDS and 34 e- without. Figure 4-a shows the predicted read noise vs. detector capacitance. Included are measured values and ranges for our 128×128, 256×256 and 1024×1024 FPAs with source follower readout. The measured levels agree with the noise predicted for the nominal design values. Based on HAWAII results, we expect that Fowler sampling will result in HAWAII-2 read noise <3 e-.

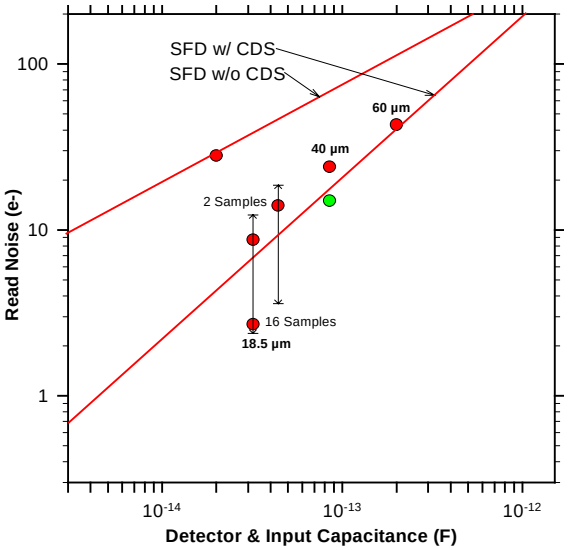


Figure 4-a. SFD FPA Read Noise: Predicted and Measured Values vs. Detector Capacitance.

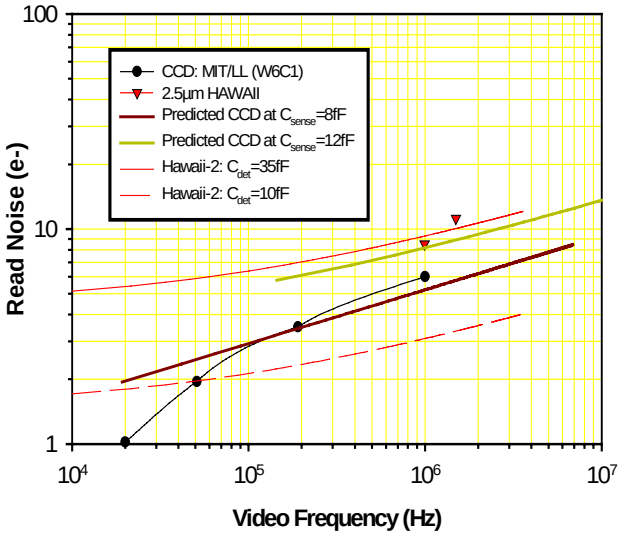


Figure 4-b. SFD FPA Read Noise: Predicted and Measured Values vs. Frequency and Detector Capacitance..

Since the multiplexer can be mated to various detector arrays including 5.5µm HgCdTe and visible silicon in addition to the baseline 2.5µm HgCdTe, the HAWAII-2 is expected to find broad use. With silicon detectors having relatively large capacitance of 10fF, for example, a visible HAWAII-2 would be superior to astronomy-grade CCDs as shown in Figure 6-b. Lowering the capacitance to the order of 1fF would enable ~1 e- read noise at higher frame rates and video frequencies than that of astronomical CCDs.

3 2048x2048 DETECTOR ARRAY OPTIONS

3.1 HgCdTe on Al2O3, SAPPHIRE (PACE-I)

Figure 5 shows one of the first 2048x2048 detector arrays processed on a 3" diameter PACE-I wafer. Only one 2048x2048 array can be processed on each wafer. The four smaller arrays at the sides of the 2048x2048 detector are 512x512 (2) and 256x256 (2) arrays for testing. Typically five wafers are processed in one lot. The unit cell size of the detector is 18 µm x 18 µm for the 2048x2048 and 512x512, and 40 µm x 40 µm for the 256x256.

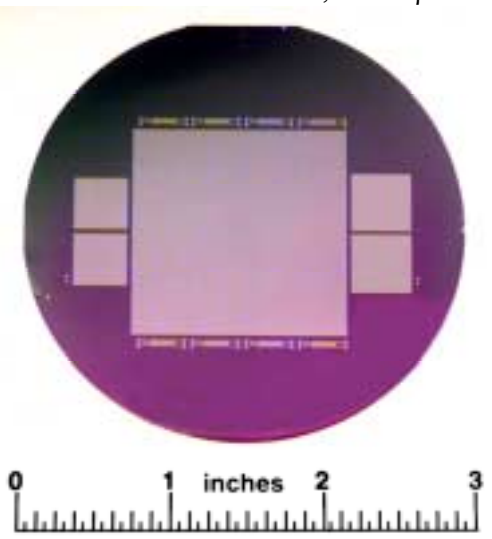


Figure 5. 2048x2048 detector array on a 3" PACE-I wafer. The arrays on the two sides are 512x512 and 256x256.

3.2 HgCdTe on CdZnTe SUBSTRATES

The MBE double layer planar heterostructure (DLPH) detector design on CdZnTe substrate is used for fabricating MWIR (5 µm cutoff) detector arrays. Dark currents are reduced due to the lower defect densities of lattice matched material system and the optimized surface passivation. 5 cm x 5 cm substrates will be used for the 2048x2048 detectors. After the processing is complete and the FPA is fabricated, the substrate is removed for reliability and visible light detection. The substrate removal has been demonstrated on 17. 3 mm x 13 mm size 640x480 FPAs and work is underway to extend this to larger formats. Visible light response with good quantum efficiency has been demonstrated after substrate removal as shown in Fig. 6.

The CdZnTe substrate strongly absorbs at wavelengths that are shorter than about 0.85µm. Without substrate removal, there would be no photon response from 0.50 µm through ~0.83 µm. The approach to achieving FPA photon response in the 0.50µm to 0.9µm band is the complete removal of the CdZnTe detector substrate. We have recently developed techniques to remove the substrate, leaving only the HgCdTe detector material on the multiplexer. The bulk substrate material is removed by a combination of mechanical polishing and wet chemical etching.

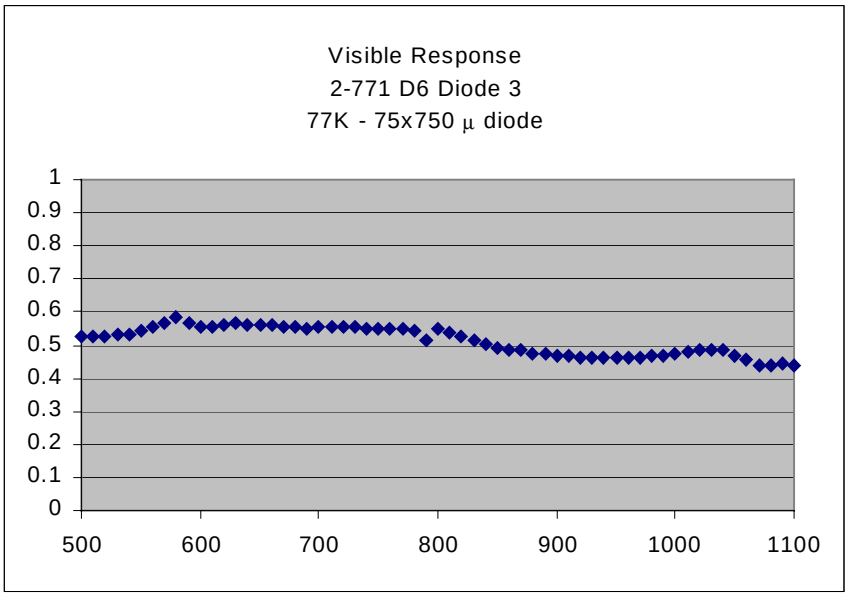
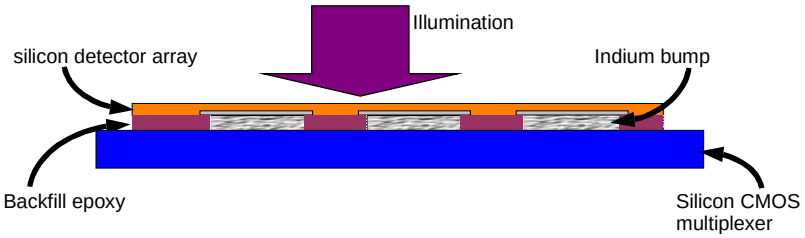


Figure 6. Quantum Efficiency of a 5.75μm cutoff HgCdTe detector array after the removal of the substrate. No AR coating was applied after substrate removal.

3.3 VISIBLE SILICON DETECTOR ARRAY

Visible-band FPA are being developed in both monolithic and hybrid format. Both approaches are based on the sub-micron CMOS readout multiplexer technology developed for IR FPAs. Figure 7 shows the baseline architecture of a hybrid visible FPA. An optimized detector array, thinned at the wafer level, is hybridized to a CMOS multiplexer. The inter-pixel gap areas, several microns high, are backfilled with space-qualified epoxy for added integrity. The resulting mechanical structure is stable and robust to harsh thermal and mechanical environments.



Figurer 7. Schematic cross-section of CMOS hybrid visible imager

Of critical importance is the fact that the bulk material will be fully-depleted at the operating voltage. The fully-depleted operational architecture results in extremely uniform photoresponse by overcoming any device thickness or spatial resistivity variations. At wavelengths less than about 800 nm, the uniformity will be limited only by the spatial non-uniformity of the transparent contact implant, and/or the AR coating. These non-uniformities over this area will be much less than 1% with current implant and thin film growth/deposition technology, and the photoresponse non-uniformity will be very small, less than 1%. At wavelengths longer than ~ 900nm, the photoresponse could begin to be affected by device thickness variations due to the much longer absorption length for these wavelengths. However, the thinning technology employed is quite capable of delivering thinned silicon wafers with total thickness variation of several μm across a 100 mm diameter.

Other key features which provide for very high quantum efficiency, in the range of 80% or higher over much of the 300 nm to 950 nm band, are the high-efficiency AR coating, the device thickness (for the longer wavelengths), and the reflecting, metallized back contact. For a fully-depleted device with an AR-coated front-

surface, the spectral quantum efficiency (QE) and front surface reflectance have been modeled using a 1-dimensional device simulator. With the optimized two-layer AR coating, the detectors will have a QE of at least 80% across the 400 nm to 900 nm band, and well over 45% at 950 nm.

We have developed 640x480 (27µm pixel) format visible FPAs based on the above architecture and have recently achieved high quantum efficiencies and low dark current. As indicated by spectral response measurement of Fig. 8, high QE responses extend down to 0.35µm wavelength and QE loss is primarily limited by the optical reflection loss, which can be readily improved by multi-layer AR-coating design. Also shown in the Fig. 8 QE histogram, is a 97.6% QE uniformity. Figure 9 shows FPA dark current vs. temperature dropping dark current density to about 0.1nA/cm^2 at 257K. The temperature dependence of the dark current agrees well with the theoretical prediction, making the visible array technology suitable for a variety of applications from ground based to space based systems.

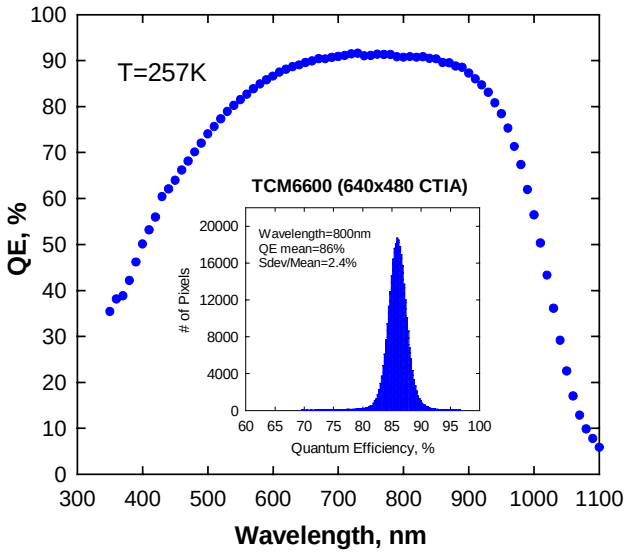


Figure 8. Relative QE histogram as measured on a 640x480 format visible FPA recently demonstrated at Rockwell

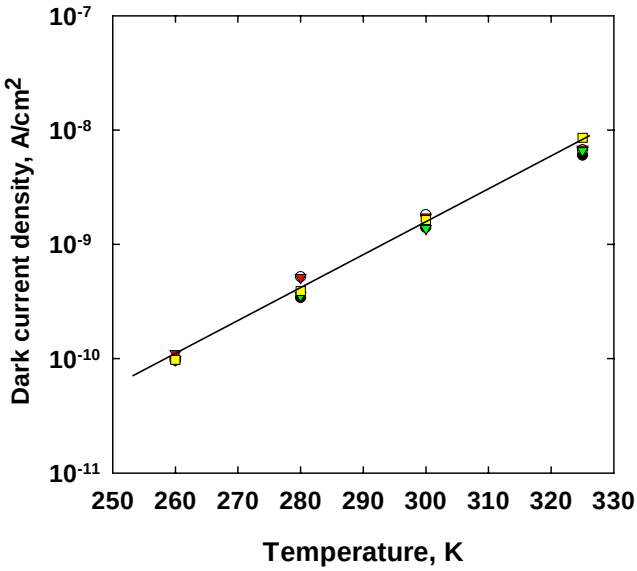


Figure 9. Dark current as measured on a 640x480 format visible FPA recently demonstrated at Rockwell

4 FOCAL PLANE ARRAY ASSEMBLY

The hybrid FPA architecture involves forming an electrical interconnect between each pixel in the detector and the multiplexer. This is done by depositing indium on each pixel of both components, and aligning and pressing together the parts on a specialized hybrid mating apparatus. We have been mating 1024x1024 FPAs for over 5 years, and have developed equipment and methods that make this a routine process. The larger die size of these arrays requires more accurate parallelism of the components to prevent open interconnects. The relatively small pixel pitch of these FPAs also places stricter limits on the lateral alignment of the die. The indium-to-indium bonding of these FPAs requires rather high loads, which demands extreme rigidity in the mating apparatus to prevent bending or lateral slip. We procured a custom mating apparatus to meet these exacting requirements, and over the past 5 years we have developed specialized methods of aligning and bonding this type of FPA.

4.1 HYBRID MATING

The detector die and multiplexer are mated together in a process designed to form a strong mechanical bond and good electrical interconnects between each detector pixel and the input to the corresponding multiplexer cell. The approach used for the HAWAII-2 is an extension of the methods successfully used to fabricate all of our

1024x1024 FPAs. Indium interconnects are deposited on each pixel of the detector and multiplexer die through thermal evaporation and lift-off. Following dicing of the wafers, the two components are aligned on our custom mating machine and pressed together to form a cold metal weld between the parts. Prior to the mating of actual detector and multiplexer die, fan-outs in the 2048x2048 format have been mated together to determine the optimum mating parameters, such as the mating load. Due to the large size of this FPA, very high loads are required to bond the hybrid, and maintaining the proper alignment of the die is challenging. The initial hybrids were mated at relatively low loads to prevent misalignment, at the detriment of the interconnection yield. The hybridization process for 2048x2048 FPAs is currently being optimized to increase detector array to multiplexer interconnect yield.

4.2 HYBRID RELIABILITY

As arrays get larger and larger, thermal cycling reliability and stress issues are important. The stress is caused by the thermal expansion mismatch between the CdZnTe or sapphire detector substrate, the silicon readout circuit and the die mounting substrate. This stress is the main cause of repetitive thermal cycling degradation in hybrid FPAs. This degradation can result in degraded detector performance, open interconnects, or complete delamination. Hence, to minimize the stress on the indium interconnects when the FPA is cooled down to the operating temperature, two methods of hybridization have been developed: the Balanced Composite Structure (BCS) design; and detector substrate removal.

We use the BCS to minimize the thermal stresses on the detectors and interconnects and extend the thermal cycling lifetime. This design places a laminate structure under the multiplexer to compress the multiplexer to match the thermal contraction of the detector. Using the BCS design, we have observed many hundreds of thermal cycles on 1024x1024 HAWAII FPAs without degradation, and we expect similar performance on the HAWAII-2 FPAs.

For very large CdZnTe substrate based FPAs, substrate removal is required to improve its thermomechanical reliability. This is expected to improve the thermomechanical reliability of the large, 2048x2048, FPA structure by leaving only the thin HgCdTe detector layer on the FPA. When cooled, the thin detector array stretches without cracking, reducing the strain on the indium interconnects. This approach may eliminate the need for the BCS, leading to a simpler overall FPA construction, allowing the detector array-hybrid structure to be directly mounted to the FPA carrier substrate. Additionally, this type of hybrid is expected to be relatively insensitive to bending induced by mounting the FPA in the dewar, which should greatly simplify the task of designing and assembling the dewar and FPA clamp assembly. The detector stress may still be an issue, and we are actively evaluating the thermal cycling reliability of this type of hybrid.

4.3 PACKAGING

The 2048x2048 array features a multiplexer nearly 4 x 4 cm, which demands a very large package. We selected a pin-grid array (PGA) package, which is commonly used for integrated circuits with hundreds of I/O lines. Although the ICs normally packaged in PGAs are rarely larger than 1 x 1 cm, the packages are made quite large to accommodate the many connections. Thus, we were able to procure a semi-custom package with a very large die attach area.

The electrical connections for the package are in the outer two rows of the 19x19 pin grid array, leaving the central connections for thermal contact. The package is inserted into a zero-insertion force socket, which allows positive electrical and thermal contact without applying stress to the ceramic package body. The thermal cooling of the package is through the central, electrically inactive, region of the socket and package. A photo of a 2048x2048 FPA in a PGA package is shown in Fig. 10.

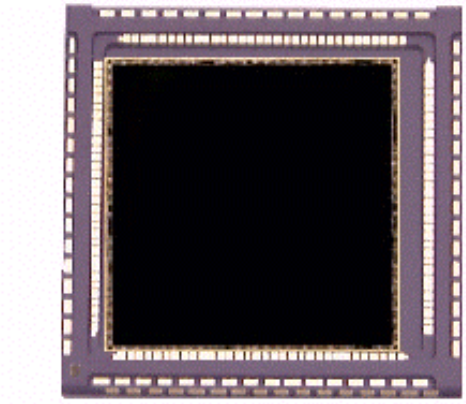


Figure 10. 2048x2048 FPA in a PGA package

5 SWIR 1024x1024 HAWAII-I RESULTS

The HAWAII 1024×1024 is the largest and most sensitive IR FPA currently available. We have delivered more than twenty, science grade HAWAII-I FPAs with 0.85-2.5 µm waveband response. The quantum efficiency spatial map for one of the arrays is shown in Figure 11. The pixel operability (pixels with quantum efficiency greater than half the mean) is 99.88%. The mean quantum efficiency is 65.4% and the non-uniformity (one sigma to mean ratio) is 4.3%. We expect the HAWAII-II FPAs to be similar in performance since the quadrants are very similar to the HAWAII-I FPAs.

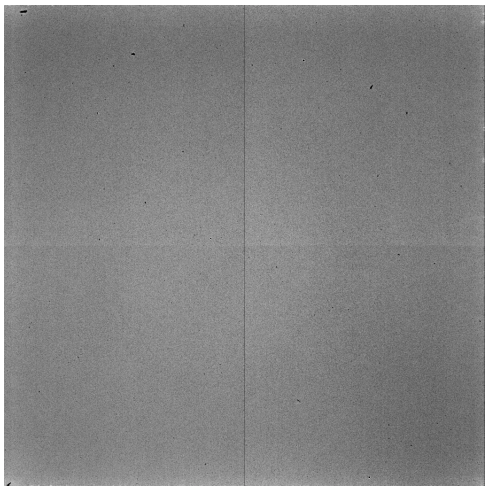


Figure 11. Quantum efficiency spatial map for a 1024x1024 HAWAII-I FPA. The mean quantum efficiency is 65.4% with a standard deviation to mean ratio of 4.3%. The pixel operability is 99.88%.

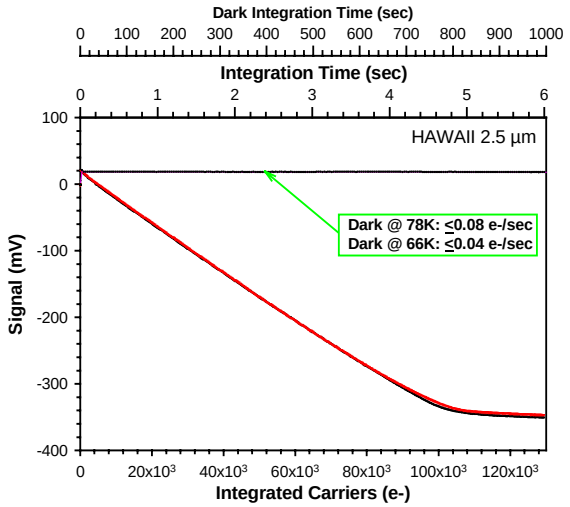


Figure 12. HAWAII pixel output vs. time under light and dark operating conditions.

Figure 12 shows the outputs from two representative HAWAII pixels vs. integration time under normal operating background and at "zero" background. Both are well-behaved and show classic SFD operation including the absence of the "reset anomaly" sometimes present in readouts with SFD input. The zero background data, obtained at 78K and 66K, show upper limits on dark current of 0.08 e-/s and 0.04 e-/s, respectively. HAWAII read noise is typically <9 e- using conventional correlated double sampling (CDS). Fowler techniques have enabled read noise <3 e-.

Figure 13 is a histogram of the quantum efficiency for a recent HAWAII. The mean quantum efficiency with K-band spectral filter is 61.5% with 5.9% rms nonuniformity and 99.987% operability. Much of the nonuniformity is related to aperture shading across the large array. We are currently working to reconfigure our dewars to minimize this testing artifact on the HAWAII and better mechanize HAWAII-2 characterization.

Figure 14 is a D* histogram for a second HAWAII FPA (9-73R-5) at a background of $5x10^9$ photons/cm^2-sec. The mean value of $1.18x10^{14}$ Jones is essentially 100% BLIP for the measured quantum efficiency (71%) and the radiometric accuracy of ±2%. One sixteenth of the full array population was arbitrarily sampled in order to take a sufficient number of frames to minimize statistical variations in calculating rms noise and better estimate operability relative to D* (normalized S/N ratio). The pixel yield of 99.87% is nearly identical to the operability measured for the full array.

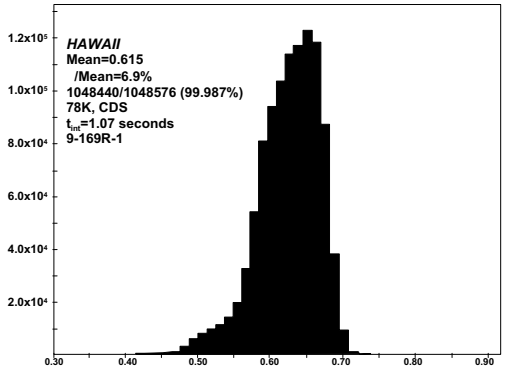


Figure 13. Quantum Efficiency Histogram for HAWAII FPA 9-169R-1.

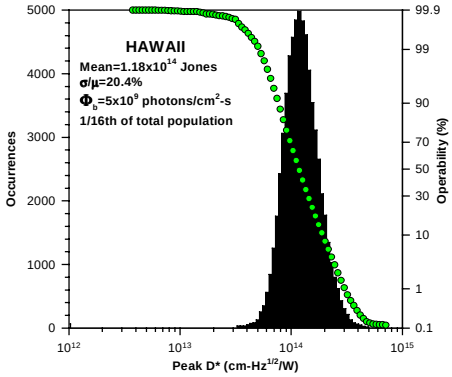


Figure 14. D* Histogram at nominal K-band irradiance for FPA 9-73R-5.

The dark current of the HAWAII-I FPAs is low at 78K. Figure 15 is a histogram of the dark current at 78K for a third HAWAII FPA, 9-173R-A2. The mean dark current is 0.0175 e-/s at 78K. The median dark current is <0.04 electrons/second. The yield of pixels with dark current <0.138 e-/s is 99.98%. The dark current will further decrease as the temperature is decreased, but is difficult to measure because of the long integration times required.

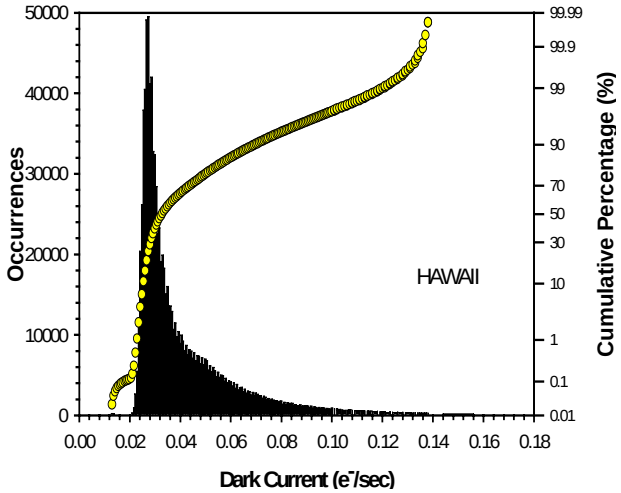


Figure 15. The dark current histogram for HAWAII-I at 78K.

6 SWIR 2048x2048 HAWAII-II RESULTS

The first 2048x2048 hybrid focal plane array has been fabricated using a 2.5μm, PACE-1 detector array. It should be noted the fabrication emphasis was on functionality and not on operability. To minimize the risk, the first assembly attempt used an engineering grade multiplexer and detector array. Engineering is underway to enhance the operability and reliability, and optimize the assembly parameters of these arrays. The upper left quadrant of this multiplexer was non-operational. The conservative mating approach to assembling the first 2048x2048 FPA resulted in numerous unconnected detectors. Subsequent FPAs will be mated using the optimized hybridization process for the 2048x2048 FPA format. Figure 16 is a QE map of the best quadrant of the FPA, and Figure 17 is the resulting QE histogram of the operational pixels in the three working quadrants. The QE histogram shows what looks like a good Gaussian distribution with a mean of 40.6%. The standard deviation over the mean indicates that the operational pixels in the FPA have good uniformity. Using the photo-conversion gain of 3.5mV/e from Table 1, a mean QE value of 40.6% was calculated for the operable pixels in the 3 functioning quadrants, yielding >75% operability. This is >2.37M operational pixels out of 3.15M pixels in the 3 functioning quadrants.

The multiplexer for these tests was operated in the basic mode with a single output per quadrant with a frame rate of less then 1Hz. The video output of the FPA showed the charging of the column bus, with pixel settling occurring in Xμs. Faster pixel rates showed the bandwidth limitation of the column bus charging effect.

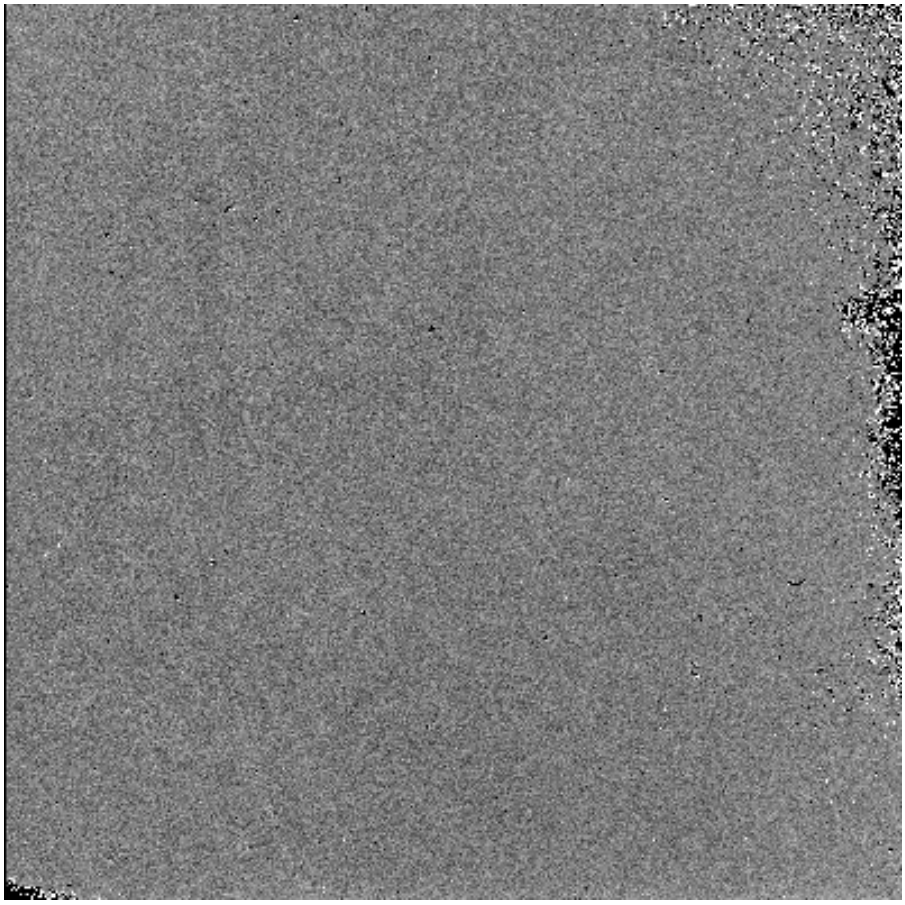


Figure 16. QE pixel map of three operational quadrants of the first HAWAII-II hybrid FPA

To cool the FPA, a thermo-mechanical connection from the cold-finger of the dewar to the pins of the PGA ceramic carrier through an indium interface was made. A temperature sensor was connected to a bare multiplexer to verify that the biased multiplexer operated at a temperature less than 1K above the 77K cold finger. With the

detector array biased at 750mV and the hybrid cooled to 78K, quantum efficiency measurements were taken, using a correlated double sampling technique. A cold "K" band filter limited the photon flux. The change in charge integrated at two different backgrounds was measured using four consecutive CDS frames.

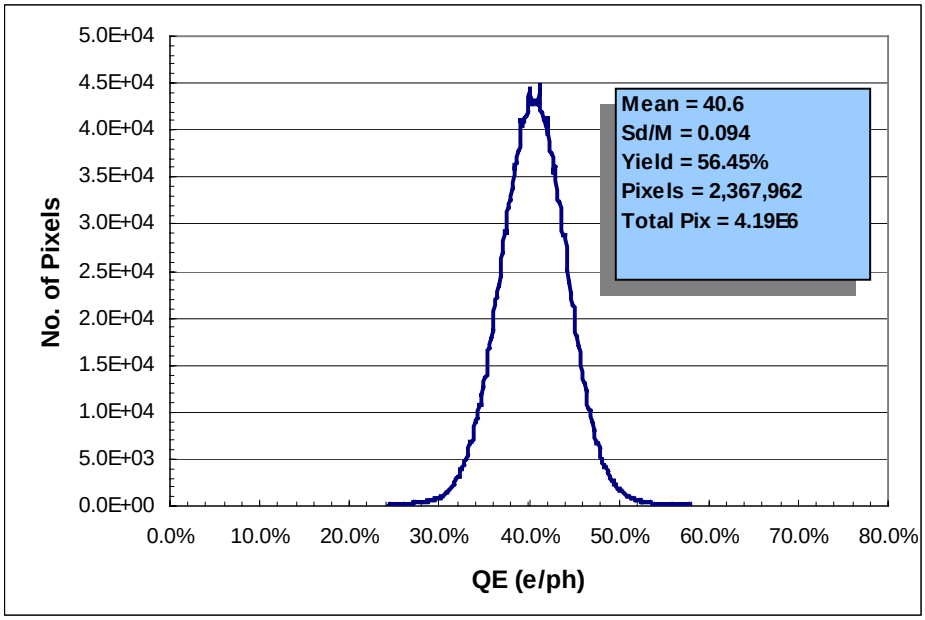


Figure 17. QE histogram measured on 2048^2 SWIR FPA

Additional tests will be performed on this FPA to fully characterize its read noise, bandwidth, dark current, D*, etc.

7 CONCLUSION

The first engineering grade 2048x2048 HAWAII-2 is currently undergoing comprehensive characterization and evaluation. This hybrid electrically functions as expected in the single output per quadrant mode of operation, with conservative hybridization, and >75% operability in the working quadrants. The operability is expected to increase to >98% in deliverable science grade FPAs. The QE, 40.6%, for this FPA has good uniformity , but is low; the QE in future FPAs is expected to increase to >55%. The dark current and read noise of this array have not been tested, but are expected to be <0.02e/sec and <10e respectively.

This engineering grade FPA was hybridized employing the BCS, for better thermo-mechanical reliability. After full characterization of this device, a 5µm cut-off FPA will be hybridized employing MCT on CZT with the CZT substrate removed. A customized pin grid array package was designed for the 2048x2048 FPA so it could be used with a zero insertion force IC socket. The thermal connection to the FPA is made through the central pins of the pin grid array package.

The substrate removal process improves the thermo-mechanical reliability and yields visible response in the band from 850nm through 400nm. Silicon visible detector arrays has been fabricated with excellent QE and dark current performance and can be mated to the HAWAII-2 multiplexer.

8 ACKNOWLEDGEMENTS

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* L. J. Kozlowski was a key contributor to the design of the HAWAII-2 FPA. He is no longer employed at the Rockwell Science Center.